AMENDMENTS TO THE CLAIMS

1-44. (Canceled)

45. (Currently amended) A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during ~~said~~ initialization processing.

wherein said first and second interrupt request signals are input to said central processing unit as a single interruption,

wherein said first and second interrupt request signals are AND'ed together to become said single interruption.

46. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said counter register is located within a random access memory at a predetermined memory address.

47. (Previously presented) A data processing apparatus as set forth in claim 45, further comprising:

bug address setting registers adapted to store said first and second bug addresses.

48. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said first bug address indicates a starting address within said program memory for a first buggy part of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program.

49. (Previously presented) A data processing apparatus as set forth in claim 48, wherein said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part.

50. (Previously presented) A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals.

51-52. (Canceled)